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FEB 27 2004
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentees: William A. Phillips
Mario Paparo
Piero Capocelli

Patent No.: 5,936,451

Title: DELAY CIRCUIT AND METHOD

Issued: August 10, 1999

Atty Dk No.: 95-L-024C3

RECEIVED
MAR 0 3 2004

Reissue Application

Applicants: William A. Phillips
Mario Paparo
Piero Capocelli

Serial No.: 09/927,426

Title: DELAY CIRCUIT AND METHOD

Filing Date: August 10, 2001

Atty Dk No.: 95-I-024C3RE (1678-41)

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited in the United States Postal Service as First Class Mail in an envelope addressed to: MS MISSING PARTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24th day of February, 2004.

Kelly Pedersen
Signature

TRANSMITTAL LETTER

TO THE COMMISSIONER FOR PATENTS:

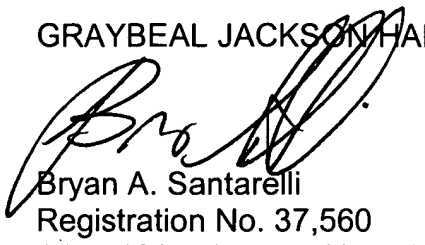
Transmitted herewith is:

A Petition to Withdraw Holding of Abandonment with Exhibit 1-6.

Because the Notice of Abandonment Under 37 CFR 1.53(f) or (g) was mailed in error, Applicants do not enclose a petition fee. However, should further payment be required to cover such fees, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP



Bryan A. Santarelli
Registration No. 37,560
155 - 108th Avenue N.E., Suite 350
Bellevue, WA 98004-5973
(425) 455-5575

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/927,426	08/10/2001	William A. Phillips	95-L-024C3 RE (1678-41)

CONFIRMATION NO. 6413

30431
STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

OIPE JC105
FEB 27 2004
PATENT & TRADEMARK OFFICE

ABANDONMENT/TERMINATION LETTER

OC000000011478648

RECEIVED
MAR 03 2004

Date Mailed: 12/12/2003

NOTICE OF ABANDONMENT UNDER 37 CFR 1.53 (f) OR (g)

The above-identified application is abandoned for failure to timely or properly reply to the Notice to File Missing Parts (Notice) mailed on 10/03/2001.

- No reply was received.

A petition to the Commissioner under 37 CFR 1.137 may be filed requesting that the application be revived.

Under 37 CFR 1.137(a), a petition requesting the application be revived on the grounds of **UNAVOIDABLE DELAY** must be filed promptly after the applicant becomes aware of the abandonment and such petition must be accompanied by: (1) an adequate showing of the cause of unavoidable delay; (2) the required reply to the above-identified Notice; (3) the petition fee set forth in 37 CFR 1.17(l); and (4) a terminal disclaimer if required by 37 CFR 1.137(d).

Under 37 CFR 1.137(b), a petition requesting the application be revived on the grounds of **UNINTENTIONAL DELAY** must be filed promptly after applicant becomes aware of the abandonment and such petition must be accompanied by: (1) a statement that the entire delay was unintentional; (2) the required reply to the above-identified Notice; (3) the petition fee set forth in 37 CFR 1.17(m); and (4) a terminal disclaimer if required by 37 CFR 1.137(d).

Any questions concerning petitions to revive should be directed to the "Office of Petitions" at (703) 305-9282.Petitions should be mailed to: Mail Stop Petitions, Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/927,426	08/10/2001	William A. Phillips	95-L-024C3 RE (1678-41)

CONFIRMATION NO. 6413

000996
GRAYBEAL, JACKSON, HALEY LLP
155 - 108TH AVENUE NE
SUITE 350
BELLEVUE, WA 98004-5901

OIPE
FEB 27 2004
PATENT & TRADEMARK OFFICE
JC105

FORMALITIES LETTER

OC000000006838108

RECEIVED
MAR 0 3 2004

Date Mailed: 10/03/2001

NOTICE TO FILE MISSING PARTS OF REISSUE APPLICATION

Filing Date Granted

An application number and filing date have been accorded to this reissue application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
 Applicant must submit $ **710** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- Total additional claim fee(s) for this application is $750.
 - **$270** for **15** total claims over 20.
 - **$480** for **6** independent claims over 3 .
- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 1590.**

A copy of this notice MUST be returned with the reply.

D. Bates

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 1 - ATTORNEY/APPLICANT COPY

EXHIBIT 1

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

Application Number:

Attachment to Paper No.:

REISSUE SUPPLEMENT
NOTICE TO FILE MISSING PARTS OF APPLICATION

This **Reissue** Supplement is an attachment to:

☐ "Notice to File Missing Parts of Application" Filing Date Granted

☐ "Notice of Incomplete Application" No filing Date Granted

The item(s) indicated below as missing must be filed within the period for reply set on the attached form to avoid abandonment.

Correction of the following is required to complete the reissue application:

☑ 1. The reissue specification has not been provided in double-column format as is required by 37 CFR 1.173(a)(1).

☐ 2. Consent of the assignee is missing. 37 CFR 1.172 requires that the reissue oath/declaration be accompanied by the written consent of all assignees.

☐ 3. Consent of the assignee is present, but is **unsigned**. A statement of consent bearing the signature of an official authorized to act on behalf of the assignee(s) must be provided.

☐ 4. Assignee's statement under 37 CFR 3.73(b) establishing ownership of the patent is missing. 37 CFR 1.72 requires that all assignees consenting to the reissue establish their ownership interest in the patent by filing in the reissue application a statement in accordance with 37 CFR 3.73(b). See MPEP Sec. 324.

☐ 5. Assignee's statement under 37 CFR 3.73(b) is present, but is **unsigned**. A 37 CFR 3.73(b) statement bearing the signature of an official authorized to act on behalf of the assignee must be provided.

D Bates

Customer Service Center
Initial Patent Examination Division (703) 308-1202

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EXHIBIT 2

POST OFFICE TO ADDRESSEE

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Date In Mo. Day Year	☐ 12 Noon ☐ 3 PM	Postage $
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No Delivery ☐ Weekend ☐ Holiday	Acceptance Clerk Initials	Total Postage & Fees $

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NO DELIVERY ☐ Weekend ☐ Holiday

Customer Signature

FROM: (PLEASE PRINT) PHONE ()

GRAYBEAL JACKSON HALEY LLP
155 108TH AVENUE N.E., SUITE 350
BELLEVUE, WA 98004-5901

1676-41

TO: (PLEASE PRINT) PHONE ()

COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

BELLEVUE, WA MAIN OFFICE
MAR 4 2002
USPS

FOR PICKUP OR TRACKING CALL 1-800-222-1811 www.usps.com EMS

GRAYBEAL JACKSON HALEY, LLP

18326

Applicants: William A. Phillips, et al.

Serial No.: 09/927,426

For: Response to Notice to File Missing Parts application filing fee & surcharge

Client: STMicroelectronics, Inc.

Docket: 1678-41

GRAYBEAL JACKSON HALEY, LLP
155 108TH AVENUE NE, SUITE 350
BELLEVUE, WASHINGTON 98004-5901
(425) 455-5575

U.S. BANK OF WASHINGTON, NA
BELLEVUE MAIN
BELLEVUE, WA 98004

19-10/1250

18326

CHECK NO.

Security features. Details on back.

DATE	AMOUNT
March 4, 2002	$1,644.00

PAY TO THE ORDER OF COMMISSIONER OF PATENTS AND TRADEMARKS

ONE THOUSAND SIX HUNDRED FORTY FOUR AND NO/100 DOLLARS***

AUTHORIZED SIGNATURE

⑈018326⑈ ⑆125000105⑆153505710423⑈

Applicants: William A. Phillips, Mario Paparo, and Piero Capocelli
Title: DELAY CIRCUIT AND METHOD
Serial No.: 09/927,426

Papers Submitted: Response to Notice to File Missing Parts of Reissue Application; First Reissue Application Declaration By The Inventors: Assent of Assignee; Certificate Under 37 CFR § 3.73(b); copy of Notice to File Missing Parts of Reissue Application; copy of Reissue Supplement Notice to File Missing Parts of Application; copy of Patent No. 5,936,451 in one column format; copy of returned postcard & Cert. Express Mail; Check No. 18326 for $1,644; Check No. 18327 for $920; Certificate of Express Mail; Request for Extension of Time

Received:

Sent: 03/04/02
Sender: kjp
Docket: 1678-41

EF 396429891 US

GRAYBEAL JACKSON HALEY, LLP

18327

Applicants: William A. Phillips, et al.

Serial No.: 09/927,426

For: Three month extension of time

Client: STMicroelectronics, inc.

Docket: 1678-41

GRAYBEAL JACKSON HALEY, LLP
155 108TH AVENUE NE, SUITE 350
BELLEVUE, WASHINGTON 98004-5901
(425) 455-5575

U.S. BANK OF WASHINGTON, NA
BELLEVUE MAIN
BELLEVUE, WA 98004

19-10/1250

18327

CHECK NO.

DATE: March 4, 2002

AMOUNT: $920.00

PAY TO THE ORDER OF: NINE HUNDRED TWENTY AND NO/100 DOLLARS***

COMMISSIONER OF PATENTS AND TRADEMARKS

AUTHORIZED SIGNATURE

MP

⑈018327⑈ ⑆125000105⑆153505710423⑈

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentees: William A. Phillips
Mario Paparo
Piero Capocelli

Patent No.: 5,936,451

Title: DELAY CIRCUIT AND METHOD

Issued: August 10, 1999

Atty Dk No.: 95-L-024C3

Reissue Application

Applicants: William A. Phillips
Mario Paparo
Piero Capocelli

Serial No.: 09/927,426

Title: DELAY CIRCUIT AND METHOD

Filing Date: August 10, 2001

Atty Dk No.: 95-I-024C3RE (1678-41)

CERTIFICATE OF MAILING OR TRANSMISSION

"Express Mail" mailing label number: EF396429891US

Date of Deposit: March 4, 2002

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR, Section 1.10 on the date indicated above and is addressed to the Commissioner for Patents, Box MISSING PARTS, Washington, D.C. 20231 by

Kelly Redmon
Signature

RESPONSE TO NOTICE TO FILE MISSING PARTS OF REISSUE APPLICATION

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

In response to the Notice to File Missing Parts of Reissue Application dated October 3, 2001, Applicants submit:

XX 1. An executed First Reissue Application Declaration By The Inventors in the above identified U.S. patent application.

XX 2. An executed Assent of Assignee.

XX 3. An executed Certificate Under 37 C.F.R. § 3.73(b) with copy of recorded Assignment.

XX 4. A copy of the NOTICE TO FILE MISSING PARTS OF REISSUE APPLICATION.

FEE COMPUTATION

Filing Fee ($740.00/$370.00)	$740.00
Surcharge Fee ($130.00/$65.00)	$130.00
Extra claim fee	$774.00
TOTAL:	$1,644.00

XX 5. Check No. 18326 for $1,644.00 filing, claim, and surcharge fees.

XX 6. A Request for Extension of Time for 3 months is enclosed with Check No. 18327 for $920.00 extension fee.

XX 7. Applicants resubmit Patent No. 5,936,451 in one column format, as requested in the Reissue Supplement Notice to File Missing Parts of Application (copy enclosed). As can be seen from the enclosed copies of the returned postcard and Certificate of Express Mailing, Patent No. 5,936,451 in one column format was submitted with this reissue application.

____ 8. Charge $_____ to Deposit Account No. _____. A copy of this sheet is enclosed.

XX 9. Please charge any additional fees or credit any overpayment to Deposit Account No. 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP

Bryan A. Santarelli
Attorney for Applicant
Registration No. 37,560
155 - 108th Avenue NE, Ste. 350
Bellevue, WA 98004
(425) 455-5575

40C 581 A10

Form PTO-1595

RECORDATION FORM COVER SHEET
PATENTS ONLY

Docket No. 954-24
U.S. Department of Commerce
Patent and Trademark Office
08/411556

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):

William Phillips
Flora Capocelli
Mario Pagano

Additional name(s) of conveying parties attached? __Yes X No

2. Name and address of receiving party(ies):

Name: SGS-THOMSON Microelectronics, Inc.

Internal Address: MS 7248

Street Address: 1310 Electronics Dr.

City: Carrollton State: TX ZIP: 75006-5039

Additional name(s) & address(es) attached? __Yes X No

3. Nature of conveyance:

X Assignment
__ Security Agreement
__ Other _____
__ Merger
__ Change of Name

Execution Date: March 9, 3, and 13, 1995

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is: March 9, 3, and 13, 1995

A. Patent Application No.(s)

B. Patent No.(s)

Additional numbers attached: __ Yes X No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Lisa K. Jorgenson
Internal Address: MS 7248

Street Address: 1310 Electronics Dr.

City: Carrollton State: TX ZIP: 75006-5039

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 3.41): $40.00
X Enclosed
__ Authorized to be charged to deposit account

8. Deposit account number:

(Attach duplicate copy of this page if paying by deposit account)

DO NOT USE THIS SPACE

9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Lisa K. Jorgenson — Lisa K. Jorgenson — 3/23/95
Name of Person Signing — Signature — Date

Total number of pages comprising cover sheet: x3 atch

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Mail documents to be recorded with required cover sheet information to:

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Washington, D.C. 20231

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RECEIVED 1995 APR 10 PM 1:19

PATENT ASSIGNMENT

WHEREAS, we, William A. Phillips, having a correspondence address 4623 Groveland Avenue, Royal Oak, MI 48073, and Mario Paparo, having a correspondence address of via Grassi, S. Giovanni Della Punta (CA) ITALY 95037, and Piero Capocelli, having a corresponding address of via Fossati 3, 20131 Milano, ITALY, respectively, have invented new and useful improvements in

A DELAY CIRCUIT AND METHOD

for which application was made for Letters Patent, said application being executed by us on the 6 day of March, 1995, and further being identified by Attorney Dockat No. 95-T-024.

WHEREAS, SGS-THOMSON MICROELECTRONICS, INC., a corporation of the State of Delaware, having a correspondence address of 1310 Electronics Drive, Carrollton, Texas 75006, is desirous of acquiring our entire right, title and interest in said application and our Letters Patent which may issue thereon:

NOW, THEREFORE, be it known by all whom it may concern that for and in consideration of One Dollar ($1.00), the receipt of which is hereby acknowledged, and other good and valuable consideration, we hereby assign to said corporation, both in and for the territory of the United States of America and the entire world our entire right, title and interest in and to said invention, patent application and any patent which may issue thereon, including all priority rights for patent applications foreign to the United States of America.

WE HEREBY covenant and agree that we will at any time, upon the request and at the expense of said corporation, execute and deliver any and all papers and do all lawful acts that may be necessary or desirable to perfect the title to said invention, applications and patents, and we authorize the Commissioner of Patents and Trademarks to issue Letters Patent to said corporation.

WE HEREBY declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

IN TESTIMONY WHEREOF, we execute this assignment on the 6 day of MARCH, 1995.

William A. Phillips

Mario Paparo

Piero Capocelli

RECEIVED
MAR 10 1995
GROUP 2800

PATENT ASSIGNMENT

WHEREAS, we, William A. Phillips, having a correspondence address 4623 Groveland Avenue, Royal Oak, MI 48073, and Mario Paparo, having a correspondence address of via Grassi, S. Giovanni Della Punta (CA) ITALY 95037, and Piero Capoccelli, having a corresponding address of via Fossati 3, 20131 Milano, ITALY, respectively, have invented new and useful improvements in

A DELAY CIRCUIT AND METHOD

for which application was made for Letters Patent, said application being executed by us on the 8+13 day of March, 1995, and further being identified by Attorney Docket No. 95-L-024.

WHEREAS, SGS-THOMSON MICROELECTRONICS, INC., a corporation of the State of Delaware, having a correspondence address of 1310 Electronics Drive, Carrollton, Texas 75006, is desirous of acquiring our entire right, title and interest in said application and our Letters Patent which may issue thereon:

NOW, THEREFORE, be it known by all whom it may concern that for and in consideration of One Dollar ($1.00), the receipt of which is hereby acknowledged, and other good and valuable consideration, we hereby assign to said corporation, both in and for the territory of the United States of America and the entire world our entire right, title and interest in and to said invention, patent application and any patent which may issue thereon, including all priority rights for patent applications foreign to the United States of America.

WE HEREBY covenant and agree that we will at any time, upon the request and at the expense of said corporation, execute and deliver any and all papers and do all lawful acts that may be necessary or desirable to perfect the title to said invention, applications and patents, and we authorize the Commissioner of Patents and Trademarks to issue Letters Patent to said corporation.

WE HEREBY declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

IN TESTIMONY WHEREOF, we execute this assignment on the 8+13 day of March, 1995.

William A. Phillips

Mario Paparo 13 March '95

Mario Paparo

8 MARCH 1995

Piero Capoccelli

MAR 28 95
RECEIVED
PATENT AND TRADEMARK OFFICE

REEL 7410 FRAME 0 1

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/927,426	08/10/2001	William A. Phillips	95-L-024C3 RE (1678-41)

CONFIRMATION NO. 6413

000996
GRAYBEAL, JACKSON, HALEY LLP
155 - 108TH AVENUE NE
SUITE 350
BELLEVUE, WA 98004-5901

FORMALITIES LETTER

OC000000006838108

Date Mailed: 10/03/2001

NOTICE TO FILE MISSING PARTS OF REISSUE APPLICATION

Filing Date Granted

An application number and filing date have been accorded to this reissue application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing. $740
 Applicant must submit $~~710~~ to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- Total additional claim fee(s) for this application is ~~$750~~ $774
 - **$270** for **15** total claims over 20.
 - ~~$480~~ for **6** independent claims over 3 . $504
- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ ~~590~~.**
 $1644.

A copy of this notice MUST be returned with the reply.

D Bates

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

10-03-01 Mail

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

Application Number:

Attachment to Paper No.:

REISSUE SUPPLEMENT
NOTICE TO FILE MISSING PARTS OF APPLICATION

This Reissue Supplement is an attachment to:

☐ "Notice to File Missing Parts of Application" Filing Date Granted

☐ "Notice of Incomplete Application" No filing Date Granted

The item(s) indicated below as missing must be filed within the period for reply set on the attached form to avoid abandonment.

Correction of the following is required to complete the reissue application:

☑ 1. The reissue specification has not been provided in double-column format as is required by 37 CFR 1.173(a)(1).

☐ 2. Consent of the assignee is missing. 37 CFR 1.172 requires that the reissue oath/declaration be accompanied by the written consent of all assignees.

☐ 3. Consent of the assignee is present, but is **unsigned**. A statement of consent bearing the signature of an official authorized to act on behalf of the assignee(s) must be provided.

☐ 4. Assignee's statement under 37 CFR 3.73(b) establishing ownership of the patent is missing. 37 CFR 1.72 requires that all assignees consenting to the reissue establish their ownership interest in the patent by filing in the reissue application a statement in accordance with 37 CFR 3.73(b). See MPEP Sec. 324.

☐ 5. Assignee's statement under 37 CFR 3.73(b) is present, but is **unsigned**. A 37 CFR 3.73(b) statement bearing the signature of an official authorized to act on behalf of the assignee must be provided.

D. Bates

Customer Service Center
Initial Patent Examination Division (703) 308-1202

ENTERED IN DOCKET
FOR: 12-3-01 Revised Ltr.
ON: 10-27-01 BY:

United States Patent [19]

Phillips et al.

[54] **DELAY CIRCUIT AND METHOD**

[75] Inventors: **William A. Phillips**, Royal Oak, Mich.; **Mario Paparo**, S. Giovanni Della Punta; **Piero Capocelli**, Milan, both of Italy

[73] Assignee: **STMicroeletronics, Inc.**, Carrollton, Tex.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/897,187**

[22] Filed: **Jul. 21, 1997**

Related U.S. Application Data

[63] Continuation of application No. 08/595,512, Feb. 1, 1996, abandoned, which is a continuation of application No. 08/411,556, Mar. 28, 1995, abandoned, which is a continuation-in-part of application No. 08/365,685, Dec. 29, 1994.

[51] Int. Cl.[6] H03K 5/13

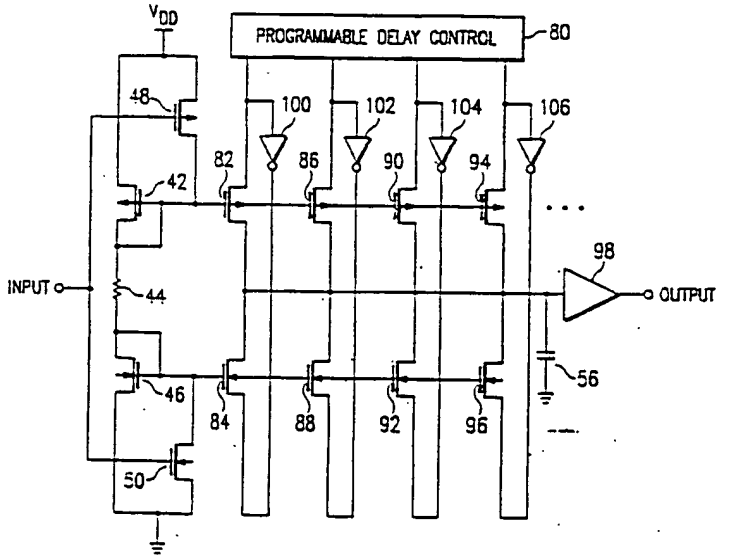
[52] U.S. Cl. 327/285; 327/288; 327/263; 327/278

[58] Field of Search 327/285, 276, 327/277, 278, 284, 281, 288, 263, 264; 365/194; 331/57

[56] References Cited

U.S. PATENT DOCUMENTS

4,740,743	4/1988	Reisinger et al.	323/316
4,806,804	2/1989	O'Leary	327/277
4,812,687	3/1989	Larson et al.	307/601



US005936451A

[11] Patent Number: 5,936,451

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[57] ABSTRACT

A reduced area delay circuit and method are disclosed. The delay circuit uses a constant current source and a constant current drain to charge and discharge a capacitor and thus control the delay time of the delay circuit. The constant current source and drain can be implemented using current mirrors formed by configuring MOSFET transistors in a common source configuration. The delay circuit method includes the steps of receiving an input signal, delaying the input signal by using a constant current source or drain in combination with a capacitor, and then buffering the voltage on the capacitor using two inverters. A programmable delay circuit is also disclosed by adding additional pairs of current mirrors to the delay circuit and selectively enabling the pairs to adjust the delay time.

15 Claims, 2 Drawing Sheets

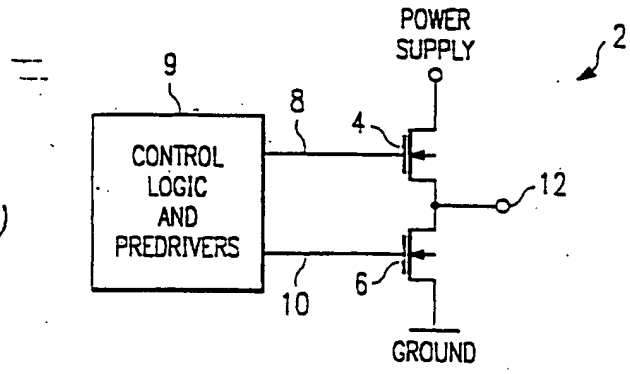


FIG. 1
(PRIOR ART)

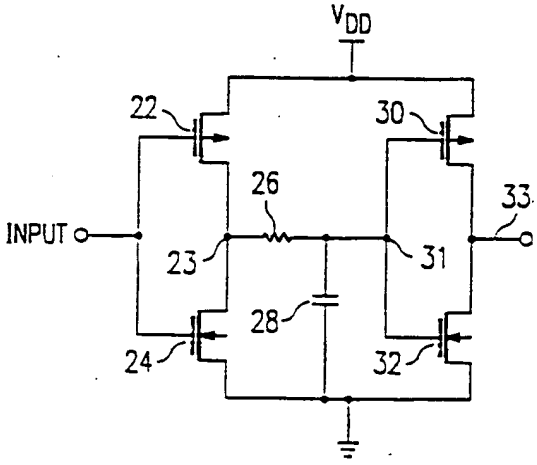
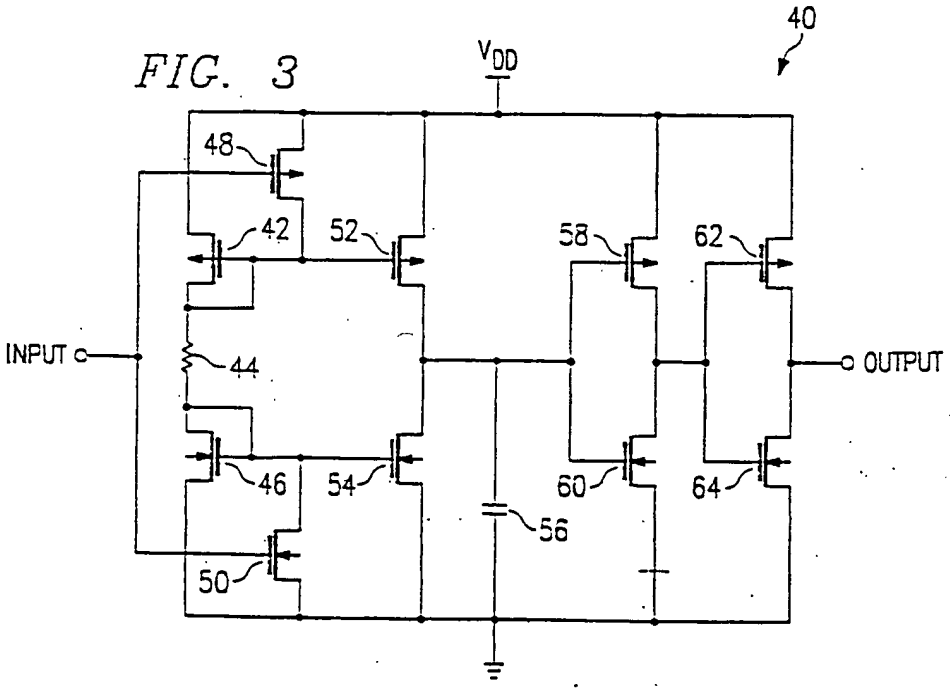


FIG. 2
(PRIOR ART)

FIG. 3



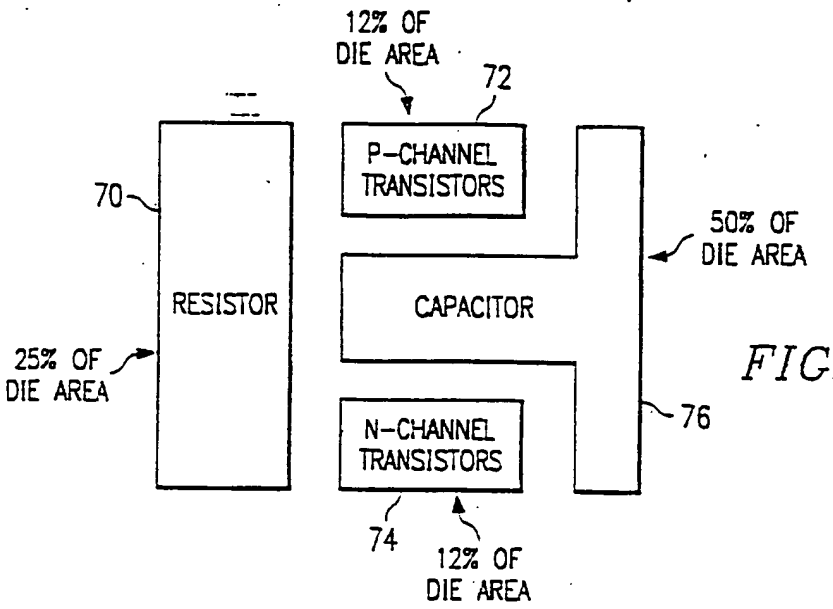
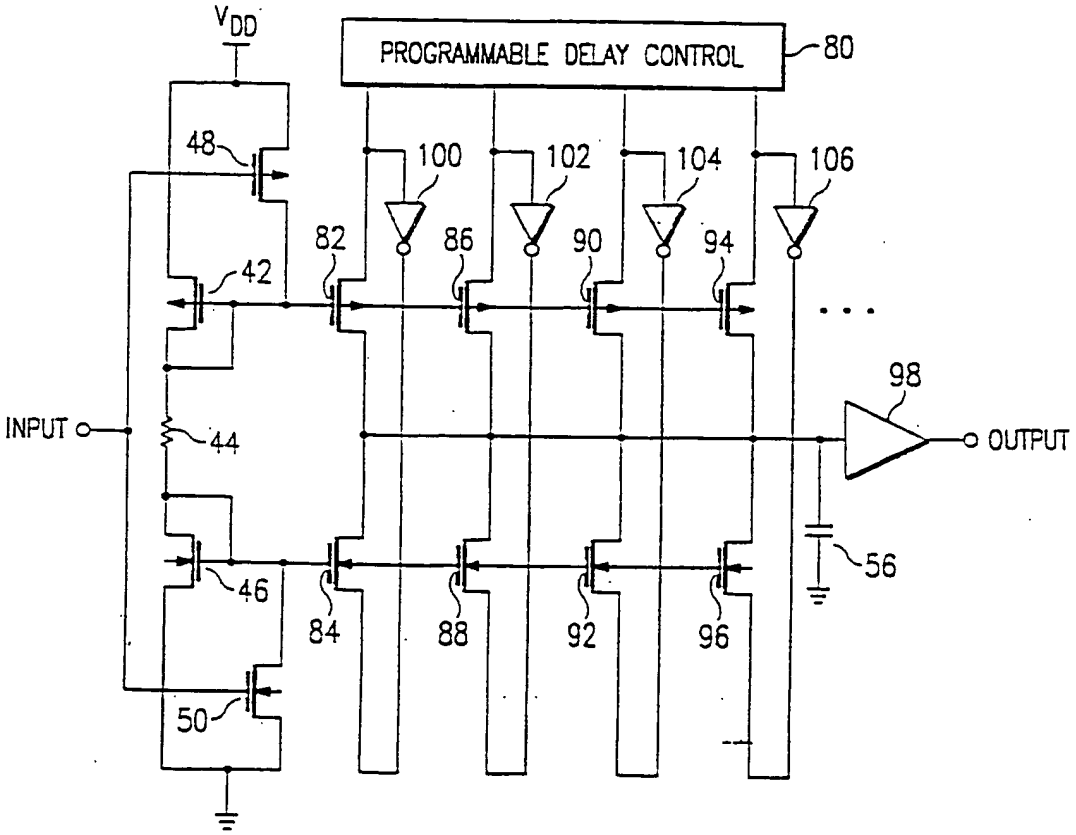

12% OF
DIE AREA
72
P-CHANNEL
TRANSISTORS
70
RESISTOR
50% OF
DIE AREA
CAPACITOR
25% OF
DIE AREA
N-CHANNEL
TRANSISTORS
76
74
12% OF
DIE AREA

FIG. 4

FIG. 5


V_{DD}
PROGRAMMABLE DELAY CONTROL
80
48
100
102
104
106
82
86
90
94
42
98
INPUT
44
OUTPUT
46
56
84
88
92
96
50

DELAY CIRCUIT AND METHOD

CROSS REFERENCE TO A RELATED APPLICATION

This is a Continuation of application Ser. No. 08/595,512, filed on Feb. 1, 1996, which has been abandoned, which is a continuation of Ser. No. 08/411,556, filed on Mar. 28, 1995, which has been abandoned; which is a Continuation In Part of Ser. No. 08/365,685, filed Dec. 29, 1994, and entitled A DELAY CIRCUIT AND METHOD, which is a pending application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to electronic circuits used to delay signals and more specifically to circuits used to delay the turn-on of a power transistor in a bridge configuration.

2. Description of the Relevant Art

The problem addressed by this invention is encountered when power transistors are used to drive a prior art bridge configuration such as in FIG. 1. The bridge configuration 2 can be used to power motors, drive solenoids, and the like. The bridge configuration 2 is characterized by the high side driver transistor 4 being connected in series to a low side driver transistor 6 across the voltage of a power supply. In this configuration, node 12 is driven to the power supply voltage when the high side transistor 4 is on and transistor 6 is off. Conversely, node 12 is sunk to ground when high side transistor 4 is off and lowside transistor 6 is on. If the high side and low side transistors are both turned off, then node 12 is at a high impedance state. However, if both high side 4 and low side 6 transistors are turned on, then the transistors are shorting the power supply voltage to ground which would draw an excessive amount of current and would damage one or both of the transistors. The bridge configuration is never used with both high side and low side drivers on at the same time because of the potentially disastrous results. Consequently, it is common to use a delay circuit as part of the control logic in the control block 9 to prevent the turn-on of one driver transistor until the other driver is turned off. In principle, one of the drivers is turned off while the other driver is turned on, but only after the delay circuit has delayed the turn-on by an amount of time which will guarantee that the other driver is in fact turned off.

FIG. 2 illustrates a prior art delay circuit 20 used in the control block 9 of FIG. 1 for delaying the turn-on of the driver transistors 4 or 6. In delay circuit 20, p-channel transistor 22 and n-channel transistor 24 form a first inverter. Similarly, p-channel transistor 30 and n-channel transistor 32 form a second inverter. The gates of transistors 22 and 24 form the inputs of the first inverter and the drain of transistor 30 and the drain of transistor 32 form the output of the second inverter. In operation, as the input signal goes from a low voltage to a high voltage, transistor 22 turns off and transistor 24 turns on. As a result, the voltage at node 23 drops from near Vdd to near ground. Consequently, the charge on capacitor 28 is drained through resistor 26 and transistor 24. The rate of discharge is determined by the size of resistor 26 and capacitor 28 as is known in the art. When the voltage on node 31 reaches approximately 2.5 volts, transistor 32 turns off and transistor 30 turns on which raises the voltage at node 33. The time delay can be approximated by the equation:

$$T_{delay}=(R26)(C28)\ln(1-Vdd/V_{threshold})$$

Therefore, the rising signal on the input of the delay circuit 20 is passed on to the output of the delay signal 33, but only after the delay created by the time constant of resistor 26 and capacitor 28. However, prior art delay circuit 20 is limited since it often requires relatively large capacitors and/or resistors to obtain long delays. The requirement of a large capacitor or resistor is undesirable since a large capacitor or resistor typically requires large amounts of silicon on an integrated circuit or requires an external connection for an external capacitor. Since the cost of a integrated circuit is directly proportional to the die size, it is desirable to reduce the size of a circuit whenever possible.

SUMMARY OF THE INVENTION

Therefore, it is an object of the invention to provide relatively long delays without requiring a large capacitor or a large resistor.

It is further an object of this invention to provide a delay circuit which provides relatively long delays and without requiring large area on an integrated circuit.

It is further an object of this invention to provide a delay circuit which reduces the cost of a delay circuit by reducing the die area necessary to implement the circuit.

These and other objects, features, and advantages of the invention will be apparent to those skilled in the art from the following detailed description of the invention, when read with the drawings and appended claims.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a schematic drawing of a prior art bridge configuration.

FIG. 2 is a schematic drawing of a prior art delay circuit.

FIG. 3 is a schematic drawing of an embodiment of a delay circuit.

FIG. 4 is a plan view of a layout of an embodiment of the delay circuit on an integrated circuit.

FIG. 5 is a schematic drawing of the delay circuit with a programmable delay control.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 3, a delay circuit 40 constructed according to an embodiment of the invention will be described. The input of the delay circuit 40 is connected to the gate of P-channel transistor 48 and to the gate of a n-channel transistor 50. The source of transistor 48 is connected to a voltage source Vdd and the drain of transistor 48 is connected to the gate of p-channel transistor 52, to the gate and drain of p-channel transistor 42, and to the first end of resistor 44. The second end of resistor 44 is connected to the drain and gate of n-channel transistor 46, to the gate of n-channel transistor 54, and to the drain of n-channel transistor 50. The sources of transistors 46, 50, and 54 are connected to a voltage reference, ground. The source of transistor 52 is connected to Vdd. The drain of transistor 52 is connected to the drain of transistor 54, to the first plate of capacitor 56, to the gate of p-channel transistor 58, and to the gate of n-channel transistor 60. The second plate of capacitor 56 is connected to ground. The source of transistor 58 is connected to Vdd. The source of transistor 60 is connected to ground. The drain of transistor 58 and the drain of transistor 60 are connected to the gate of p-channel transistor 62 and to the gate of n-channel transistor 64. The source of transistor 62 is connected to Vdd. The source of transistor 64 is connected to ground. The drain of transistor 62 is con-

nected to the drain of transistor 64, the connection thereof forms the output of the delay circuit 40. Although the construction of this circuit is described using MOSFET transistors, it is understood in the art that a similar circuit can be constructed using bipolar transistors, and the like.

In operation, an input signal is received at the gates of transistors 48 and 50. If the input signal is at a low voltage, transistor 48 turns on which allows for transistors 46 and 54 to conduct a constant current through transistor 54. The constant current through transistor 54 discharges capacitor 56. Conversely, capacitor 56 is charged when the input signal is at a high voltage since this high input voltage turns transistor 48 off and turns transistor 50 on. Therefore, transistors 46 and 54 are held off while transistors 42 and 52 are turned on. Thus, transistor 52 charges capacitor 56 with the constant current source formed by transistor 42, resistor 44, and transistor 52. The voltage on capacitor 56 buffered to the output by two inverters formed with transistors 58, 60, 62, and 64. In short, an input signal is received by transistors 48 and 50, delayed by the constant current sources or drains in combination with the capacitor, and then buffered by two inverters to the output of the delay circuit 40.

More specifically, transistors 42, 52 and 50 combine with resistor 44 to form a constant current source when the input to the delay circuit is at a high voltage. In this state, transistor 50 draws current through resistor 44 which turns on the current mirror formed by transistors 42 and 52. In the preferred embodiment, Vdd is about 5 volts and R44 is approximately 84 Kohms which defines the current through transistor 42 at about 40 microamps. Transistor 42 has an w/l (area) of 180/9 and transistor 52 has an w/l (area) of 9/9. Thus, the current through transistor 42 is approximately 20 times the current through transistor 52. Thus the current in transistor 52 is approximately 2 microamps. This constant current charges capacitor 56 when the input voltage is high. In general, the time delay can be approximately described as

$$\text{time delay} = (\text{switch voltage}/V_{R44})\ (C56)\ (R44)\ (\text{current ratio})$$

where:

switch voltage=the switch voltage for the inverter

V_{R44}=the voltage drop across R44

C56=the capacitance of capacitor 56

R44=the resistance of resistor 44

current ratio=the current ratio of the applicable current mirror.

In an embodiment, a 10 picofarad capacitor, 84 kilo-ohm resistor, and current ratio of 20 are used which yields a delay of approximately (2.5 v/4 v) (10 pF) (84 k) (20)=10.5 microseconds. (Note that the voltage drop across resistor 44 is reduced from Vdd by the voltage drop across the transistors in the current path, which in this case totals to around 1 volts.)

Conversely, transistors 48, 46, and 54 combine with resistor 44 to form a constant current drain for discharging capacitor 56. When the input of delay circuit 40 is at a low voltage, transistor 50 is off and transistor 48 is on. This allows current to flow through transistor 48 and resistor 44, thus, turning on transistors 46 and 54. With an 84 kohm resistor and 5 volt Vdd, the current through transistor 46 is approximately equal to 40 microamps. Transistor 46 has 20 times the area as transistor 54 so that the current through transistor 54 is about 2 microamps. Therefore, capacitor 56 is discharged at the rate of 2 microamps which creates a delay of about 10.5 microseconds when the input of delay circuit is low.

Transistors 58 and 60 are configured to invert the voltage on the capacitor 56. When the voltage on the gates of transistors 58 and 60 are low, the voltage on output is low and vice versa. Transistors 62 and 64 are also configured as an inverter with the gates configured as the input and the drain of transistor 62 connected to the drain of transistor 64 to form the output of the inverter. The first and second inverter form the output stage of the delay circuit and buffer the voltage on the capacitor to the output of the delay circuit 40. It is understood that numerous circuits can be used for buffering voltages without departing from the spirit and scope of the invention.

The embodiment of the invention offers the advantage providing a delay which over 12 times longer than the delay created by a prior art circuit using the same resistor and capacitor value. Alternatively, this embodiment of the invention creates the equivalent delay, but uses a resistor and/or capacitor which is approximately 12 times smaller than is required by the prior art circuit to achieve the same time delay.

FIG. 4 shows the layout of the embodiment and illustrates that 75% of the area required to implement the embodiment is used by the resistor and capacitor. The layout includes resistor 70, p-channel transistors 72, n-channel transistors 74, and capacitor 76. It can be noted that the layout is for five p-channel transistors, five n-channel transistors, one 84 kilo-ohm resistor, and one 10 picofarad capacitor and yields a 10.5 microsecond delay. The prior art delay circuit in FIG. 2 requires 4 transistors instead of 6 but only provides a delay of around 823 nanoseconds or would require a capacitor or resistor which over 12 times larger to yield the same delay. The layout in FIG. 4 shows that the extra transistors needed to implement the embodiment of the invention use much less area than the area needed to increase the resistance or capacitance by 12 times. Consequently this embodiment of the invention uses much less area than the prior art even though the invention requires 10 transistors (as compared to 4 transistors) because the transistors use much less area than capacitor or resistor which would be required. Therefore, the present invention provides relatively long delays without requiring large capacitors or resistors, without requiring a large area on an integrated circuit, and, thus, at a reduced cost relative to the prior art.

FIG. 5 discloses another embodiment which adds programmability to the delay circuit. This embodiment is constructed by having the source of p-channel MOSFET transistor 42 connected to Vdd and having its drain connected to a first end of resistor 44. The second end of resistor 44 is connected to the drain of n-channel MOSFET transistor 46. P-channel MOSFET transistor 48 has a source connected to Vdd and a drain connected to the gate of transistor 42. The drain of n-channel MOSFET transistor 50 is connected to the gate of transistor 46. The sources of transistors 46 and 50 are connected to ground. The gate of transistor 48 is connected to the gate of transistor 50, the connection of which forms the input for the circuit. The gate of transistor 42 is connected to the gates of p-channel MOSFET transistors 82, 86, 90, and 94. The gate of transistor 46 is connected to the gates of n-channel MOSFET transistors 84, 88, 92 and 96. The sources of transistors 82, 86, 90, and 94 are connected to programmable delay control circuit 80. The drains of transistors 82, 84, 86, 88, 90, 92, 94, and 96 are connected to each other and the first plate of capacitor 56. The input of inverter 100 is connected to the source of transistor 82 and the output of inverter 100 is connected to the source of transistor 84. Similarly, the inputs of inverters 102, 104, and 106 are connected to the sources of transistors 86, 90, and

94, respectively. Likewise, the outputs of inverters 102, 104, and 106 are connected to the sources of transistors 88, 92, and 96, respectively. The second plate of capacitor 56 is connected to ground. The output of buffer amplifier 98 is the output of the circuit. The programmable delay control circuit 80 can be constructed using many common digital circuits including input/output device, RAM memory, ROM memory, EPROM, EEPROM, and the like.

In operation, this embodiment operates in an analogous manner to the previous embodiment, but with the added feature that capacitor 56 can now be charged or discharged by one or more pairs of current mirrors. Transistors 48 and 50 are the input transistors; transistors 42 and 46 are the bias transistors; transistors 82, 86, 90, and 94 are the constant-current source transistors; and transistors 84, 88, 92, and 96 are the constant-current drains, for this embodiment.

More specifically, an input signal enters the circuit through the gate of transistor 48 which turns on transistor 42. Since the gate of transistor 42 is connected to the gates of transistors 82, 86, 90, and 94, transistor 42 provides the bias voltage for transistors 82, 86, 90, and 94 such that the current flow in the respective transistor is proportional (mirrored) to the current through transistor 42. However, transistors 82, 86, 90, and 94 will only be turned on if programmable delay control circuit 80 has enabled one of those transistors by providing the source of the respective transistor with a positive voltage. Therefore, the rate of delay or the rate of charging capacitor 56 is controlled by the programmable delay control circuit 80 and the relative ratios of transistors 42 to transistors 82, 86, 90, and 94. Inversely, when the input signal goes low, transistor 50 turns on bias transistor 46 which thereby provides the bias voltage to turn on transistors 84, 88, 92, and 96 to remove the charge from capacitor 56. Again, transistors 84, 88, 92, and 96 will not drain any current from capacitor 56 unless the transistors have been enabled by programmable delay control circuit 80 providing a sufficiently low voltage to the respective transistors drain. In this disclosure, it is assumed that the enable signals from the programmable delay control signal are digital in nature with sufficient current drive to drive the MOSFET transistors.

It will be clear to persons skilled in the art that additional transistor pairs can be added to the circuit to increase the range of programmability. Four transistor pairs are disclosed for illustrative purposes and could easily be modified to less pairs or more pairs by persons skilled in the art. Additionally, persons skilled in the art can vary the ratio of the current mirrors to further increase the range of programmability. By adjusting the current mirror ratios and/or increasing the number of transistor pairs persons skilled in the art can easily design a programmable delay which meets a given design criteria for versatility as well as flexibility.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

We claim:

1. A delay circuit comprising:

a plurality of current mirror current sources, with each current mirror current source having an enable input, having an input for receiving an input signal and having a constant current output for providing a constant current responsive to the input signal;

a plurality of current mirror current drains, with each current mirror current drain having an enable input,

having an input for receiving the input signal, and having a constant drain output for providing a constant current responsive to the input signal;

a programmable delay control circuit having a plurality of enable signals, each signal connected to a current mirror current source and current mirror current drain such that the programmable delay control circuit selectively enables a pair of current mirror current source and drain;

a fixed capacitor having a first plate and a second plate, the first plate of the capacitor connected to the constant current outputs of the plurality of current mirror current sources and to the constant drain outputs of the plurality of current drains, the second plate connected to a voltage reference, with each current mirror current source having a current path between a corresponding enable signal of said programmable delay control circuit and the first plate of said capacitor and with, each current mirror current drain having a current path between the corresponding enable signal of said programmable delay control circuit and the first plate of said capacitor; and

an output stage having an input connected to the first plate of the capacitor and having an output for providing an output responsive to the voltage on the capacitor

wherein a delay on the rising edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current sources to change an overall current source current provided by the plurality of current mirror current sources to the first plate of the capacitor, and

wherein a delay on the falling edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current drains to change an overall current drain current provided by the plurality of current mirror current drains to the first plate of the capacitor.

2. The delay circuit of claim 1 wherein the programmable delay control circuit comprises a digital circuit.

3. The delay circuit of claim 2 wherein the digital circuit comprises programmable memory circuit.

4. The delay circuit of claim 3 wherein the programmable memory circuit comprises a programmable read only memory.

5. The delay circuit of claim 4 wherein the programmable read only memory comprises a EEPROM.

6. The delay circuit of claim 3 wherein the programmable memory circuit comprises a FLASH memory.

7. A delay circuit comprising:

a first input transistor having a control element for receiving an input signal, and having a current path with a first end connected to a voltage source and a second end;

a second input transistor having a control element for receiving the input signal, and having a current path with a first end and a second end connected to a voltage reference;

a first bias transistor having a current path with a first end connected to the voltage source, having second end, and having a control element, wherein the second end is connected to the control element and to the second end of the current path of the first input transistor;

a resistor having a first end connected to the second end of said first bias transistor and having a second end;

a second bias transistor having a current path from the second end of said resistor to the voltage reference, and having a control element connected to the second end of said resistor and to the first end of the current path of said second input transistor;

a capacitor having a first plate and having a second plate connected to the voltage reference;

an output stage having an input connected to the first plate of said capacitor and having an output;

a programmable delay control circuit having a plurality of enable outputs;

a plurality of constant-current sources, each constant current source of the plurality of constant-current sources having a current path between a corresponding enable output of said programmable delay control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said first bias transistor such that the current flowing in the first bias transistor is proportionately mirrored in the current path of each constant-current source of the plurality of constant-current sources, responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current source; and

a plurality of constant-current drains, each constant current drain of the plurality of constant-current drains having a current path between the corresponding enable output of said programmable delay control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said second bias transistor such that the current flowing in the second bias transistor is proportionately mirrored in the current path of each constant-current drain of the plurality of constant-current drains, responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current drain.

8. The delay circuit of claim 7 wherein said programmable delay control circuit comprises a digital circuit.

9. The delay circuit of claim 8 wherein the digital circuit comprises programmable memory circuit.

10. The delay circuit of claim 9 wherein the programmable memory circuit comprises a programmable read only memory.

11. The delay circuit of claim 10 wherein the programmable read only memory comprises a EEPROM.

12. The delay circuit of claim 9 wherein the programmable memory circuit comprises a FLASH memory.

13. A delay circuit comprising:

a plurality of current mirror current elements, with each current mirror current element having an enable input, having an input for receiving an input signal and having a constant current output for providing a constant current responsive to the input signal;

a programmable delay control circuit having a plurality of enable signals, each enable signal connected to the plurality of current mirror current elements so as to selectively enable a current mirror current element of the plurality of current mirror current elements;

a fixed capacitor having a first plate and a second plate, the first plate of the capacitor connected to the constant current outputs of the plurality of current mirror current elements, the second plate connected to a voltage reference, with each current mirror current element having a current path between a corresponding enable signal of said programmable delay control circuit and the first plate of said capacitor; and

an output stage having an input connected to the first plate of the capacitor and having an output for providing an output responsive to the voltage on the capacitor,

wherein a delay on an active edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current elements to change an overall current provided by the plurality of current mirror current elements to the first plate of the capacitor.

14. The delay circuit of claim 13, wherein the active edge of the input signal is a rising edge of the input signal and the plurality of current mirror current elements are a plurality of current mirror current sources, and a delay on the rising edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current sources to change an overall current source current provided by the plurality of current mirror current sources to the first plate of the capacitor.

15. The delay circuit of claim 13, wherein the active edge of the input signal is a falling edge of the input signal and the plurality of current mirror current elements are a plurality of current mirror current drains, and a delay on the falling edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current drains to change an overall current drain current provided by the plurality of current mirror current drains to the first plate of the capacitor.

* * * * *

Applicants: William A. Phillips, Mario Paparo, and Piero Capocelli

Title: DELAY CIRCUIT AND METHOD

Papers Submitted: Reissue Patent Application Transmittal; First Preliminary Amendment; Assent of Assignee; Certificate Under 37 CFR § 3.73(b); First Reissue Application Declaration By The Inventors; copy of Patent No. 5,936,451 in one column format; copy of Patent No. 5,936,451; Certificate of Express Mail

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Original Patent

Patentees: William A. Phillips
Mario Paparo
Piero Capocelli

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Issued: August 10, 1999

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Reissue Application

Applicants: William A. Phillips
Mario Paparo
Piero Capocelli

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First Preliminary Amendment
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentees: William A. Phillips
Mario Paparo
Piero Capocelli

Patent No.: 5,936,451

Title: DELAY CIRCUIT AND METHOD

Issued: August 10, 1999

Atty Dk No.: 95-L-024C3

Reissue Application

Applicants: William A. Phillips
Mario Paparo
Piero Capocelli

Serial No.: 09/927,426

Title: DELAY CIRCUIT AND METHOD

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REQUEST FOR EXTENSION OF TIME

March 4, 2002

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Applicants respectfully request that the shortened statutory period for response to the outstanding Notice to File Missing Parts of Reissue Application mailed October 3, 2001, now set to expire on December 3, 2001, be extended three (3) months to expire on March 3, 2002 (Sunday).

Enclosed is our check no. 18327 in the amount of $920.00 (3 months).

Please charge any additional fees or credit overpayment to Deposit Account No. 07-1897.

Respectfully submitted,

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Papers Submitted: Response to Notice to File Missing Parts of Reissue Application; First Reissue Application Declaration By The Inventors: Assent of Assignee; Certificate Under 37 CFR § 3.73(b); copy of Notice to File Missing Parts of Reissue Application; copy of Reissue Supplement Notice to File Missing Parts of Application; copy of Patent No. 5,936,451 in one column format; copy of returned postcard & Cert. Express Mail; Check No. 18326 for $1,644; Check No. 18327 for $920; Certificate of Express Mail; Request for Extension of Time

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EXHIBIT 3

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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/929,425	08/10/2001	William A. Phillips	95-L-024C3 RE (1678-41)

000996

GARYBEAL, JACKSON, & HALEY LLP

155 – 108TH AVENUE NE. SUITE 350

BELLEVUE, WA. 98001-98001-5901

Date Mailed: 04/25/2002

SECOND NOTICE

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

Correction of the following is required to complete the reissue application:

X The reissue specification has not been provided in double-column format as is required by 37 CFR 1.173(a)(1). **A surcharge is not required when supplying this item.**

Consent of the assignee is missing. 37 CFR 1.172 requires that the reissue oath/declaration be accompanied by the written consent of all assignees. Until this item is supplied, the oath/declaration remains defective; thus, **payment of the surcharge ($130 for large entity; $65 for small entity) under 37 CFR 1.53(f) and 37 CFR 1.16(e) is required in addition to the supplying of this item. See MPEP § 1410.01.**

Consent of the assignee is present, but is unsigned. A statement of consent bearing the signature of an official authorized to act on behalf of the assignee(s) must be provided, to comply with 37 CFR 1.172. Until this item is supplied, the oath/declaration remains defective; thus, **payment of the surcharge ($130 for large entity; $65 for small entity) under 37 CFR 1.53(f) and 37 CFR 1.16(e) is required in addition to the supplying of this item. See MPEP § 1410.01.**

Assignee's statement under 37 CFR 3.73(b) establishing ownership of the patent is missing. 37 CFR 1.72 requires that all assignees consenting to the reissue establish their ownership interest in the patent by filing in the reissue application a statement in accordance with 37 CFR 3.73(b). See MPEP § 324. Until this item is supplied, the oath/declaration remains defective; thus, **payment of the surcharge ($130 for large entity; $65 for small entity) under 37 CFR 1.53(f) and 37 CFR 1.16(e) is required in addition to the supplying of this item. See MPEP § 1410.01.**

Assignee's statement under 37 CFR 3.73(b) is present, but is unsigned. A 37 CFR 3.73(b) statement bearing the signature of an official authorized to act on behalf of the assignee must be provided. Until this item is supplied, the oath/declaration remains defective; thus, **payment of the surcharge ($130 for large entity; $65 for small entity) under 37 CFR 1.53(f) and 37 CFR 1.16(e) is required in addition to the supplying of this item. See MPEP § 1410.01.**

EXHIBIT 4

*A copy of this notice **MUST** be returned with the reply.*

Office of Initial Patent Examination (703)308-1202

Applicants: William A. Phillips, Mario Paparo, and Piero Capocelli
Title: DELAY CIRCUIT AND METHOD
Serial No.: 09/927,426

Papers Submitted: Response to Second Notice to File Missing Parts of Nonprovisional Application; copy of U.S. Patent No. 5,936,451 in double-column format; copy of Certificate of Express Mail & returned postcard; copy of Second Notice to File Missing Parts of Nonprovisional Application; copy of First Reissue Application Declaration By The Inventors; Certificate of Mailing

Sent: 6-25-02
Sender: kjp
Docket: 1678-41

EXHIBIT 5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentees: William A. Phillips
Mario Paparo
Piero Capocelli

Patent No.: 5,936,451

Title: DELAY CIRCUIT AND METHOD

Issued: August 10, 1999

Atty Dk No.: 95-L-024C3

Reissue Application

Applicants: William A. Phillips
Mario Paparo
Piero Capocelli

Serial No.: 09/927,426

Title: DELAY CIRCUIT AND METHOD

Filing Date: August 10, 2001

Atty Dk No.: 95-I-024C3RE (1678-41)

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited in the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on this 25th day of June, 2002.

Kelly Pedersen
Signature

RESPONSE TO SECOND NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

In response to the Second Notice to File Missing Parts of Nonprovisional Application dated April 25, 2002, Applicants submit:

___ 1. An executed First Reissue Application Declaration By The Inventors in the above identified U.S. patent application.

___ 2. An executed Assent of Assignee.

___ 3. An executed Certificate Under 37 C.F.R. § 3.73(b) with copy of recorded Assignment.

XX 4. A copy of the SECOND NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION.

FEE COMPUTATION

Filing Fee ($740.00/$370.00)	$N/A
Surcharge Fee ($130.00/$65.00)	$N/A
Extra claim fee	$N/A
TOTAL:	$-0-

____ 5. Check No. _____ for $_____ filing, claim, and surcharge fees.

____ 6. A Request for Extension of Time for ____ months is enclosed with Check No. _____ for $_____ extension fee.

XX 7. Applicants resubmit Patent No. 5,936,451 in double column format, as requested in the Second Notice to File Missing Parts of Nonprovisional Application (copy enclosed). As can be seen from the enclosed copies of the returned postcard and Certificate of Express Mailing, Patent No. 5,936,451 in double column format was submitted with this reissue application.

XX 8. Please change the correspondence address to that indicated on the First Reissue Application Declaration By The Inventors, which was filed with the application, as well as with the Response to Notice to File Missing Parts. A copy of the First Reissue Declaration is enclosed.

____ 9. Charge $_____ to Deposit Account No. _____. A copy of this sheet is enclosed.

XX 10. Please charge any additional fees or credit any overpayment to Deposit Account No. 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP

Bryan A. Santarelli
Attorney for Applicant
Registration No. 37,560
155 - 108th Avenue NE, Ste. 350
Bellevue, WA 98004
(425) 455-5575

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY OF COMMERCE AND
NER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/929,425	08/10/2001	William A. Phillips	95-L-024C3 RE (1678-41)

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A copy of this notice MUST be returned with the reply. 19-Day

Office of Initial Patent Examination (703)308-1202

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentees: William A. Phillips
Mario Paparo
Piero Capocelli

Patent No.: 5,936,451

Title: DELAY CIRCUIT AND METHOD

Issued: August 10, 1999

Atty Dk No.: 95-L-024C3

Reissue Application

Applicants: William A. Phillips
Mario Paparo
Piero Capocelli

Serial No.:

Title: DELAY CIRCUIT AND METHOD

Filing Date:

Atty Dk No.: 95-L-024C3RE (1678-41)

CERTIFICATE OF MAILING OR TRANSMISSION

"Express Mail" mailing label number: EF271983974US

Date of Deposit: August 10, 2027

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR, Section 1.10 on the date indicated above and is addressed to the Commissioner for Patents, Box PATENT APPLICATION, Washington, D.C. 20231 by

Signature

Enclosures:

Reissue Patent Application Transmittal
Certificate Under 37 C.F.R. 3.73(b) (not signed)
Assent of Assignee (not signed)
Reissue Application Declaration by the Inventors (not signed)
First Preliminary Amendment
Copy of Patent No. 5,936,451 (regular)
Copy of Patent No. 5,936,451 (in one column form)
Return postcard

Applicants: William A. Phillips, Mario Paparo, and Piero Capocelli

Title: DELAY CIRCUIT AND METHOD

Papers Submitted: Reissue Patent Application Transmittal; First Preliminary Amendment; Assent of Assignee; Certificate Under 37 CFR § 3.73(b); First Reissue Application Declaration By The Inventors; copy of Patent No. 5,936,451 in one column format; copy of Patent No. 5,936,451; Certificate of Express Mail

Received:

11000 U.S. PTO
09/927426
08/10/01

Sent: 8-10-01
Sender: kjp
Docket: 1678-41

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentees: William A. Phillips
Mario Paparo
Piero Capocelli

Patent No.: 5,936,451

Title: DELAY CIRCUIT AND METHOD

Issued: August 10, 1999

Atty Dk No.: 95-L-024C3

Reissue Application

Applicants: William A. Phillips
Mario Paparo
Piero Capocelli

Serial No.: 09/927,426

Title: DELAY CIRCUIT AND METHOD

Filing Date: August 10, 2001

Atty Dk No.: 95-I-024C3RE (1678-41)

FIRST REISSUE APPLICATION DECLARATION BY THE INVENTORS

As a below named inventor, I hereby declare:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are listed below) of the subject matter that is claimed in patent number 5,936,451 granted August 10, 1999, and for which a reissue patent is sought on the invention entitled:

DELAY CIRCUIT AND METHOD

the specification of which

- ☐ is attached hereto.
- ☑ was filed on August 10, 2001 as reissue application number 09/927,426 and was amended on _____ (if applicable). If the filing date, amendment date, or reissue application number are not included when I execute this Declaration, I authorize the below appointed attorney(s) and/or agents(s) to insert the filing date, amendment date, or reissue application number when they become available.

I have reviewed and understand the contents of the above–identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all that apply.)

- ☐ by reason of a defective specification or drawing.
- ☑ by reason of the patentee claiming less than he had the right to claim in the patent.
- ☐ by reason of other errors.

Errors upon which reissue is based are described as follows:

I believe that "a plurality of current mirror current sources" and "a plurality of current mirror current drains" in claim 1, "a plurality of constant-current sources" and "a plurality of constant-current drains" in claim 7, and "a plurality of current mirror current elements" in claim 13 overly narrow the issued claims because an embodiment of our invention can include one current source, one current drain, or one mirror current element. Therefore, we have added new claims 16 – 35.

All errors corrected in this reissue application arose without any deceptive intention on my part.

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: all attorneys associated with Customer Number 30431.

Correspondence Address: Direct all communications about the application to:

Lisa K. Jorgenson
STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, Texas 75006-5039
Phone: (972) 466-6000
Fax: (972) 466-7044

I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof.

I do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country before my invention thereof.

I do not know and do not believe that the claimed invention was ever patented or made the subject of an inventor's certificate issued prior to the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns.

I do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country more than one year prior to the filing date of the original U.S. application.

I do not know and do not believe that the claimed invention was ever in public use or on sale in the United States of America more than one year prior to the filing date of the original U.S. application.

I hereby claim the benefit of priority, under 35 U.S.C. § 119 and 35 U.S.C. § 120, of any foreign application(s) for patent or inventor's certificate on which priority was claimed in the above-identified issued patent.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon, or any patent to which this declaration is directed.

William A. Phillips — Full Name of Inventor

BRITISH — Citizenship

4708 HOLLY TREE DRIVE DALLAS TX 75287 — Residence

Post Office Address (if different from Residence)

William A. Phillips — Inventor's Signature

2/13/02 — Date

Mario Paparo — Italian

Full Name of Inventor — Citizenship

Via Grassi n 1 - 95037 San Giovanni La Punta (Catania) Italy

Residence

Post Office Address (if different from Residence)

Mario Paparo — 21st Nov. 2001

Inventor's Signature — Date

Piero Capocelli — Italian

Full Name of Inventor — Citizenship

via Fossati 3 20131 Milano - Italy

Residence

Post Office Address (if different from Residence)

[signature] — December 3rd 2001

Inventor's Signature — Date

Applicants: William A. Phillips, Mario Paparo, and Piero Capocelli
Title: DELAY CIRCUIT AND METHOD
Serial No.: 09/927,426

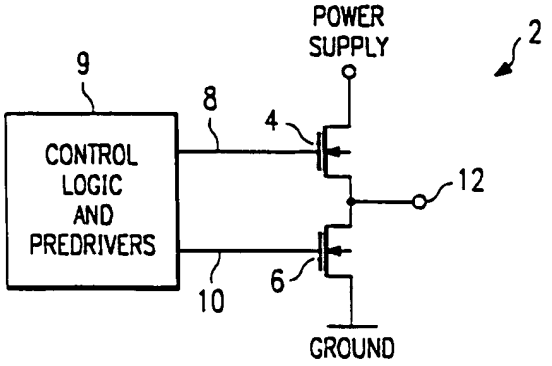
Papers Submitted: Response to Second Notice to File Missing Parts of Nonprovisional Application; copy of U.S. Patent No. 5,936,451 in double-column format; copy of Certificate of Express Mail & returned postcard; copy of Second Notice to File Missing Parts of Nonprovisional Application; copy of First Reissue Application Declaration By The Inventors; Certificate of Mailing



Sent: 6-25-02
Sender: kjp
Docket: 1678-41

EXHIBIT 6

FIG. 1
(PRIOR ART)



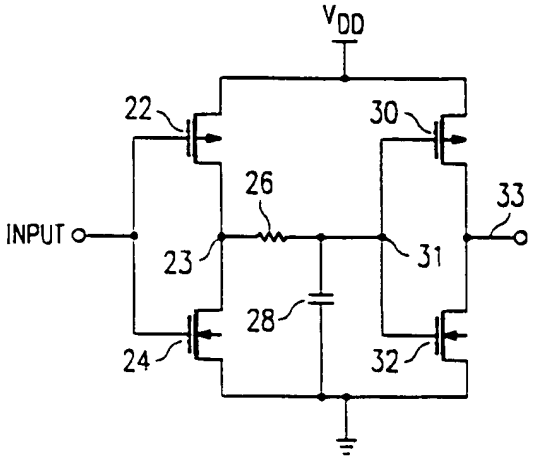
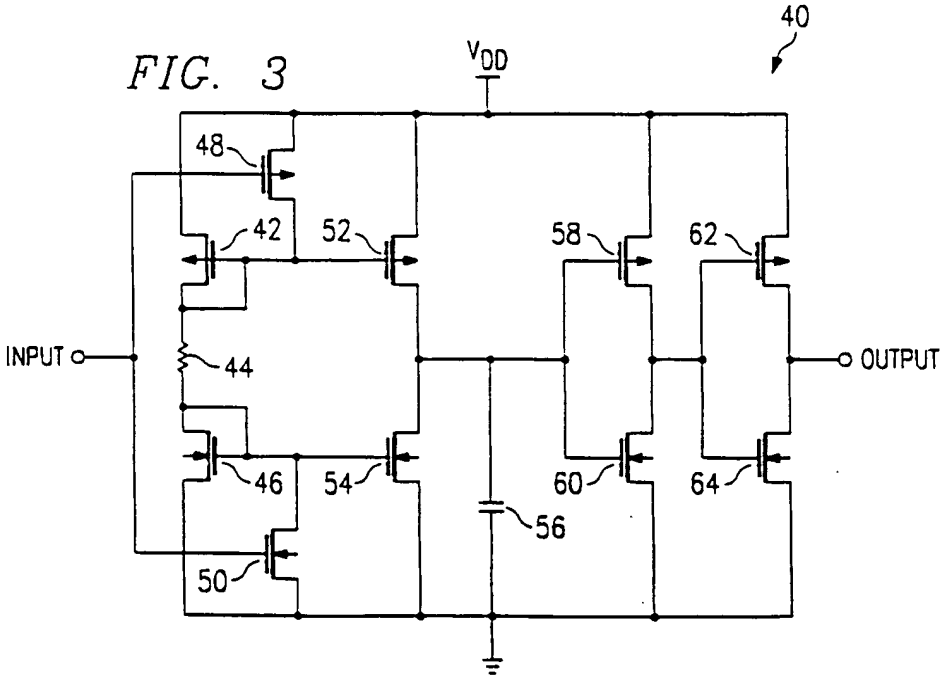


FIG. 2
(PRIOR ART)

FIG. 3



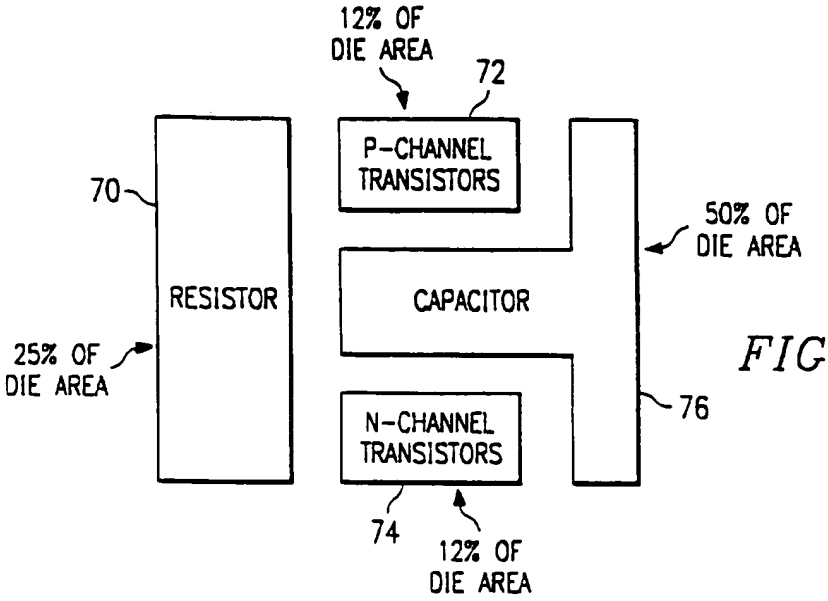
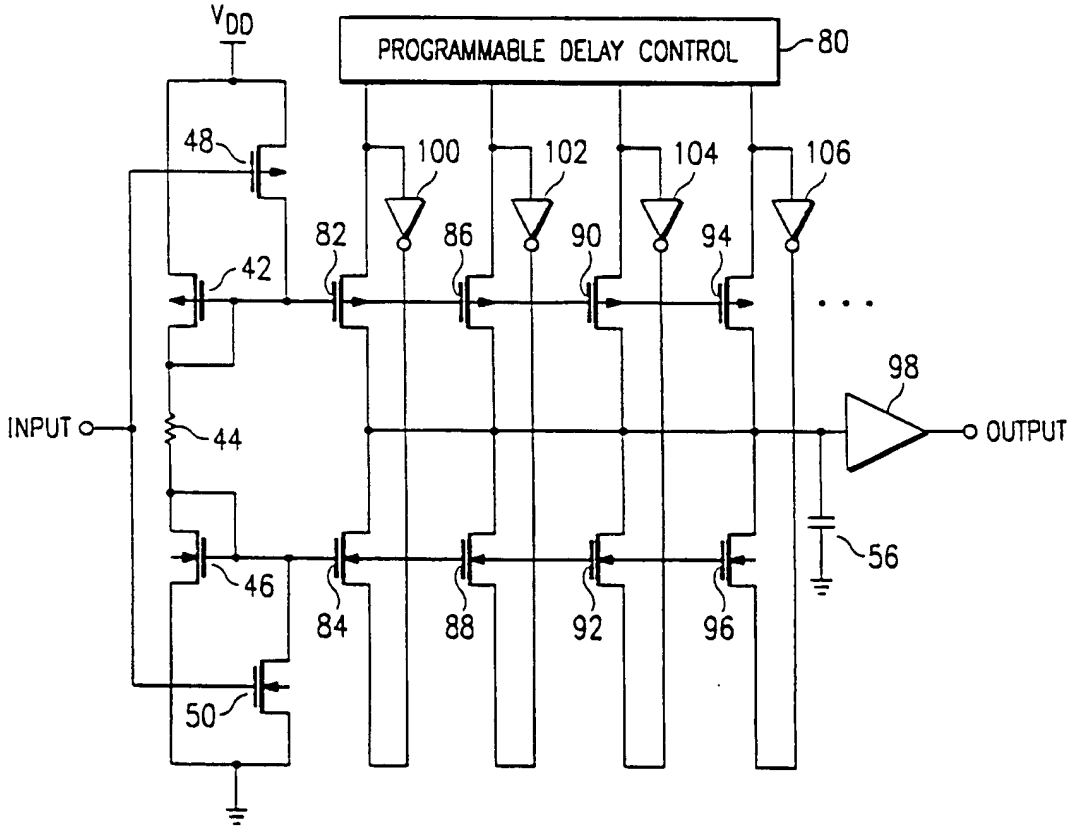

12% OF
DIE AREA
72
P-CHANNEL
TRANSISTORS
70
RESISTOR
50% OF
DIE AREA
CAPACITOR
25% OF
DIE AREA
76
N-CHANNEL
TRANSISTORS
74
12% OF
DIE AREA

FIG. 4

FIG. 5


V_{DD}
PROGRAMMABLE DELAY CONTROL
80
48
100
102
104
106
82
86
90
94
42
98
INPUT
44
OUTPUT
56
46
84
88
92
96
50